Claims

[c1] 1.A method of suppressing parasitic device characteristics in a finFET, comprising the steps of:

a)forming a finFET so as to define a plurality of reentrant corners formed where each horizontal surface meet a vertical surface;

depositing a layer of a material over said finFET; and

removing said layer so as to leave a portion of said layer substantially only at each of said plurality of reentrant corners so as to form a plurality of spacers.

[c2] 2.A method according to claim 1, wherein the finFET comprises a source and a drain and the method further comprises the step of doping each of said source and said drain subsequent to the step of removing said layer of material so as to leave a portion of said layer only substantially at each of said plurality of reentrant corners.

[c3] 3.A method according to claim 2, wherein the step of doping comprises implanting ions by ion implantation.

[c4] 4.A method according to claim 1, wherein said material is a silicon dioxide.

[c5] 5.A method according to claim 1, wherein the step of removing said layer includes etching said layer using reactive ion etching.

[c6] 6.A method according to claim 1, wherein said finFET includes at least one fin formed using a hardmask positioned atop said at least one fin, said fin having a source region and a drain region, the method further comprising the step of removing substantially all of said hardmask from said source and drain regions not located underneath corresponding ones of said plurality of spacers.

[c7] 7.A method according to claim 1, wherein said finFET includes at least one fin, the method further comprising the step of undercutting at least a portion of said fin.

[c8] 8.A method of forming a finFET, comprising the steps of:
a)forming a fin having a source portion, a drain portion and a channel portion extending between said source portion and said drain portion, each of said source portion and said drain portion having an upper surface and a length extending away from said channel portion;
forming a gate at said channel portion so as to define a first reentrant corner between said upper surface of said source and said gate and a second reentrant corner between said upper surface of said drain and said gate;
forming a first spacer proximate said first reentrant corner and second spacer proximate said second reentrant corner, said first spacer extending a distance away from said gate in a direction along said source less than said length of said

source and said second spacer extending a distance away from said gate in a direction along said drain a distance less than said length of said drain; and

subsequent to forming said first and second spacers, doping each of said source and drain.

[c9] 9.A method according to claim 8, wherein the step of doping comprises implanting ions by ion implantation.

[c10] 10.A method according to claim 8, wherein the step of forming said first and second spacers includes depositing a layer of a material over said fin and said gate and removing a portion of said layer so as to form said first and second spacers.

[c11] 11.A method according to claim 10, wherein said material comprises a deposited oxide.

[c12] 12.A method according to claim 11, wherein said material comprises silicon nitride.

[c13] 13.A method according to claim 10, wherein the step of removing a portion of said layer includes etching said layer by reactive ion etching.

[c14] 14.A method according to claim 8, wherein the step of forming said fin includes anisotropically etching a substrate except in a region masked by a hardmask located atop said fin.

[c15] 15.A method according to claim 14, further comprising the

step of removing substantially all of said hardmask from said source and drain portions not located underneath first and second spacers.

[c16] 16.A method according to claim 8, further comprising the step of undercutting at least a portion of said fin.

[c17] 17.A device, comprising:

a)an integrated circuit formed on a substrate and comprising a plurality of FETs wherein at least some of said plurality of FETs are finFETs each comprising:

i)a fin having a source portion, a drain portion and a channel portion extending between said source portion and said drain portion, each of said source portion and said drain portion having an upper surface and a length extending away from said channel portion;

a gate located at said channel portion so as to define a first reentrant corner between said upper surface of said source portion and said gate and a second reentrant corner between said upper surface of said drain portion and said gate; and

a first spacer proximate said first reentrant corner and second spacer proximate said second reentrant corner, said first spacer extending a distance away from said gate in a direction along said source portion less than said length of said source portion and said second spacer extending a distance away from said gate in a direction along said drain portion a

distance less than said length of said drain portion.

[c18] 18.A device according to claim 17, further comprising a hardmask remnant located between said first spacer and said upper surface of said source and between said second spacer and said upper surface of said drain.

[c19] 19.A device according to claim 17, wherein said fin has a base portion attached to said substrate, said substrate including an undercut region located beneath at least a portion of said fin, said finFET further comprising a third spacer formed adjacent said base portion, said undercut portion containing at least a portion of said third spacer.

[c20] 20.A device according to claim 17, wherein each of said first and second spacer comprises silicon dioxide.